IN THE CLAIMS

Please amend Claims 1-20 as follows:

1. (Previously Presented) A transceiver for a serial data bus, in which the transceiver is connected via a transmission line and a receiving line to a protocol controller, which manages a data bus protocol and which is coupled to the lines of the data bus, and in which the transceiver comprises means for error management which means supplies an error signal when it recognizes that the data bus lines are active and that the receiving line simultaneously signals an inactive bus.

2. (Previously Presented) A transceiver for a serial data bus, in which the transceiver is connected via a transmission line and a receiving line to a protocol controller which manages a data bus protocol, and is coupled to the lines of the data bus, and in which the transceiver comprises means for error management, which means comprise a timer circuit which triggers an error signal when the transmission line is active for a longer period than a predetermined time interval, which error signal is cancelled when both the transmission line is inactive and the receiving line is active.

3. (Previously Presented) A transceiver as claimed in claim 1, characterized in that the means for error management switch off the so supplied error signal when the receiving line is active.

4. (Previously Presented) A transceiver as claimed in claim 1, characterized in that, responsive to the error signal, a bus transmission stage in the transceiver is switched to the inactive state.

5. (Previously Presented) A transceiver as claimed in claim 1, characterized in that the error signal is signaled external to the transceiver by means of an error line.

6. (Previously Presented) A transceiver as claimed in claim 1, characterized in that a control line is provided, whose activation resets the means for error management, switching the error signal to the inactive state.

7. (Previously Presented) A transceiver as claimed in claim 1, characterized in that the means for error management comprise a flip-flop which, in the set state, supplies the error signal.

8. (Previously Presented) A transceiver as claimed in claim 7, characterized in that the means for error management comprise a first AND gate whose output signal is applied to the flip-flop and which sets the flip-flop when the data bus lines are active and the receiving line simultaneously is inactive.

9. (Previously Presented) A transceiver as claimed in claim 2, characterized in that the timer circuit sets a flip-flop when the transmission line is active for a longer period than a predetermined time interval.

10. (Previously Presented) A transceiver as claimed in claim 8, characterized in that a second AND gate is provided whose inputs receive signals from the receiving line and the transmission line and which resets the flip-flop and thus switches the error signal to an inactive state when the transmission line is inactive and the receiving line is active.

11. (Previously Presented) A transceiver as claimed in claim 1, characterized in that said error signal has the effect that the transceiver no longer acts actively on the data bus

12. (Previously Presented) A transceiver as claimed in claim 1, characterized in that means for error management comprise a timer circuit which triggers an error signal when the transmission line is active for a longer period than a predetermined time interval, which error signal is cancelled when both the transmission line is inactive and the receiving line is active.

13. (Previously Presented) A transceiver as claimed in claim 5, characterized in that the error signal is signaled external to the transceiver to an application having priority over the protocol controller.

14. (Previously Presented) A transceiver as claimed in claim 2, characterized in that the predetermined time interval is in accordance with a minimal time interval ensured by the data bus protocol for an inactive state of the data bus.

15. (Previously Presented) A transceiver for a serial data bus having data bus lines, the transceiver coupled to a protocol controller via a transmission line and a receiving line, the transmission line carrying a signal generated from the protocol controller indicative of data bus protocol respecting a writing process on the data bus lines, and the receiving line carrying a signal indicative of activity on the data bus lines, the transceiver comprising:

error management logic that monitors the signals of the transmission line and receiving line, the error management logic including determination logic that, responsive to the monitored signals, determines whether the data bus lines are in one state when the receiving line simultaneously signals the bus is in an opposite state, and the error management logic including signal logic that, responsive to said determination, provides an error signal.

16. (Previously Presented) A transceiver as claimed in claim 15, wherein the signal logic generates an active error signal responsive to the determination logic determining that the data bus lines are active when the receiving line simultaneously is inactive.

17. (Previously Presented) A transceiver as claimed in claim 16, wherein the signal logic generates an inactive error signal responsive to the determination logic determining that the transmission line is inactive and receiving line is active.

18. (Currently Amended) A transceiver as claimed in claim 16, further comprising ~~timer logic~~ a timer, the timer generating a timer signal responsive to the transmission line being active for a time period that is longer than a predetermined time interval, and wherein the signal logic, responsive to said timer signal, provides an error signal.

19. (Previously Presented) A transceiver as claimed in claim 18, wherein the timer generates the timer signal responsive to the transmission line being active for a time period which is longer than a predetermined time interval that is in accordance with a time interval ensured by the data bus protocol for an inactive state to arise on the data bus.

20. (Previously Presented) A transceiver as claimed in claim 18, wherein the signal logic generates an active error signal responsive to the timer signal indicating that the predetermined time interval is exceeded.